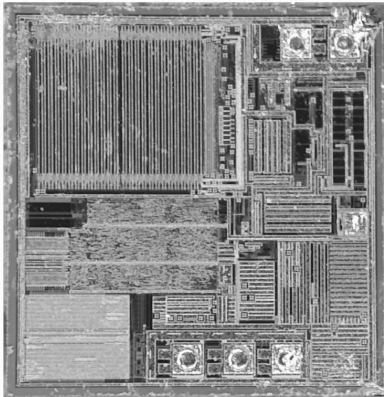
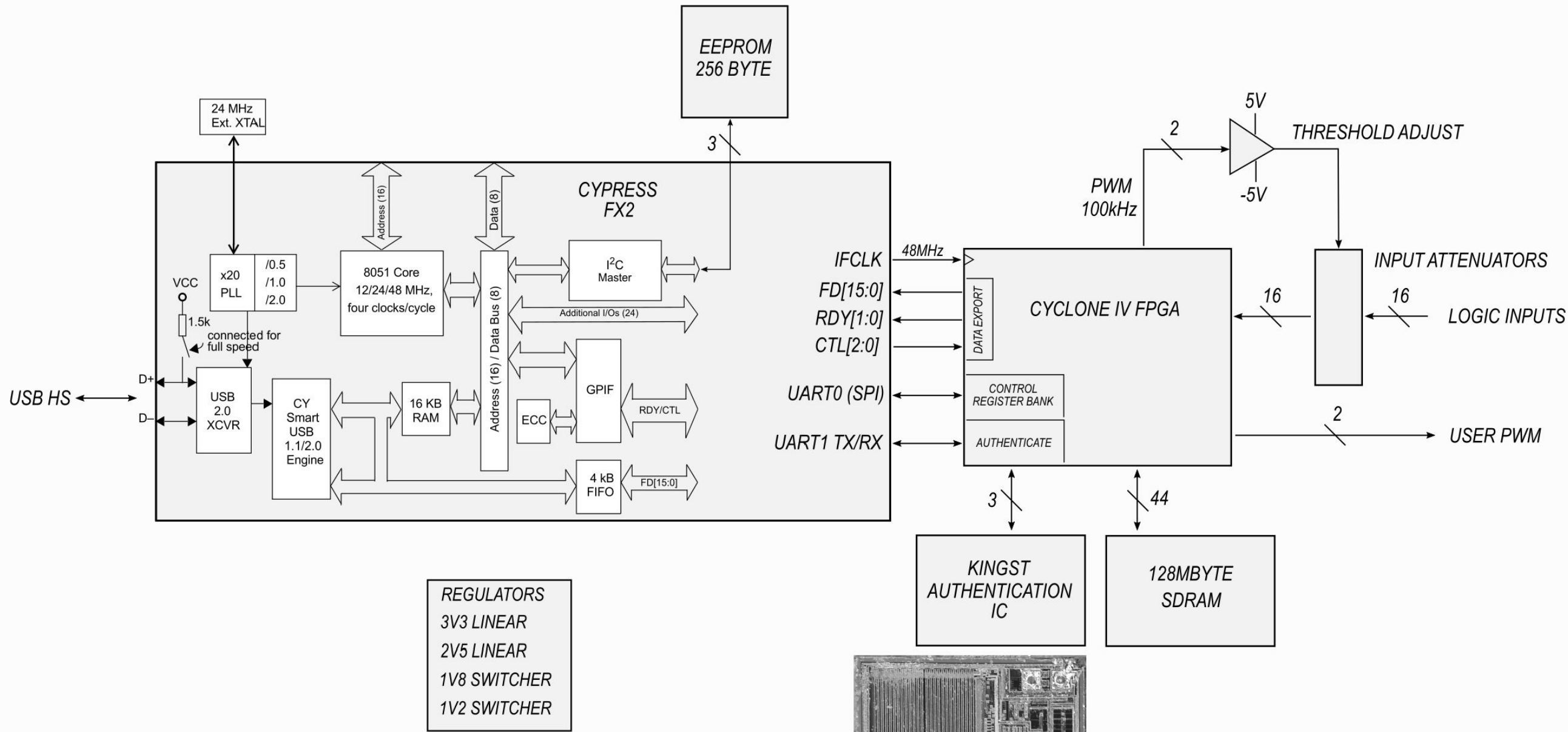


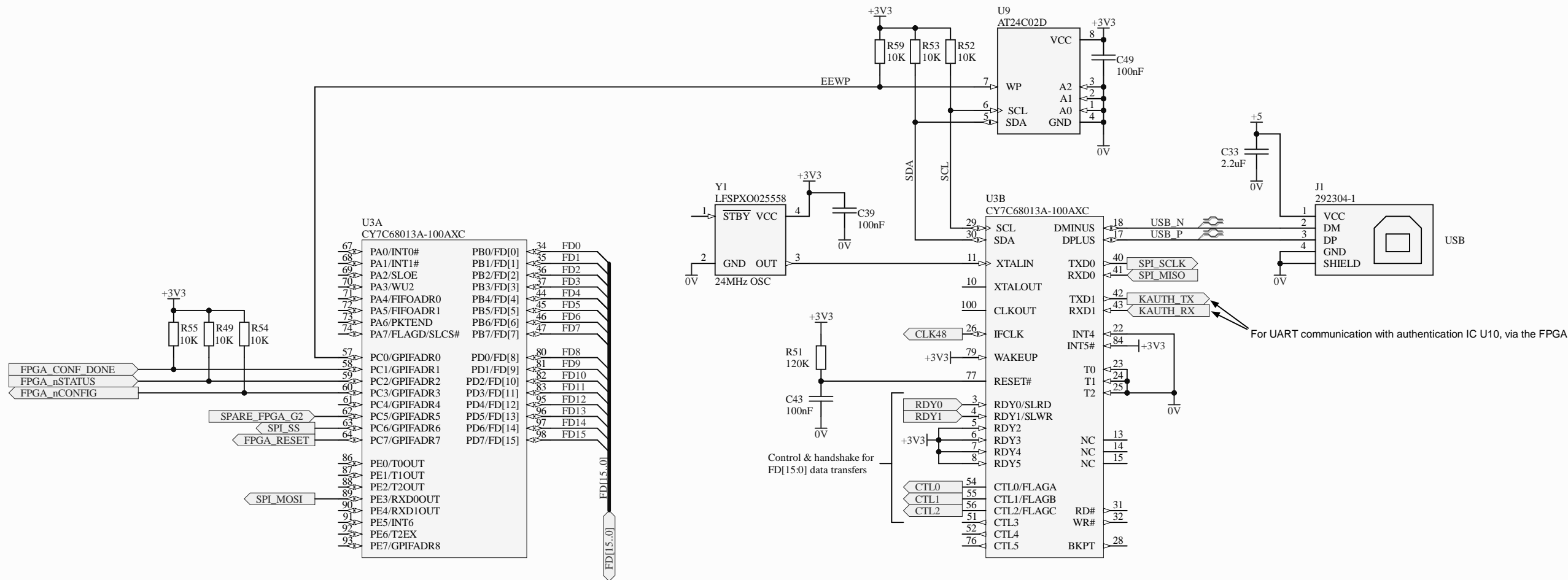
Title LA1016 / LA2016 PCB V1.3.0				
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Parts:		
U1	EP4CE6F17C8N	Altera Cyclone IV FPGA E Family 6272 Cells **
U2,4,5,7	PDWL050019	TVS array
U3	CY7C68013A-100AXC	Cypress FX2 USB Microcontroller
U6,U8	SGM2019	SG-Micro Adjustable linear regulator
U9	AT24C02	ATmel EEPROM 256 bytes
U10	MCU	Kingst authentication device, small MCU, not identified.
U11	K4T1G164QG-BCF8	Samsung 1Gb DDR2 SDRAM 84 FBGA DDR2-1066
U12, U13	SGM6013	SG-Micro Adjustable switching regulator
U14	SGM8272	SG-Micro Dual op-amp
U15	TPS60403	Texas Charge pump voltage inverter
** FPGA uses the same die as the next larger device, so more cells are actually available and can be programmed, although not guaranteed		



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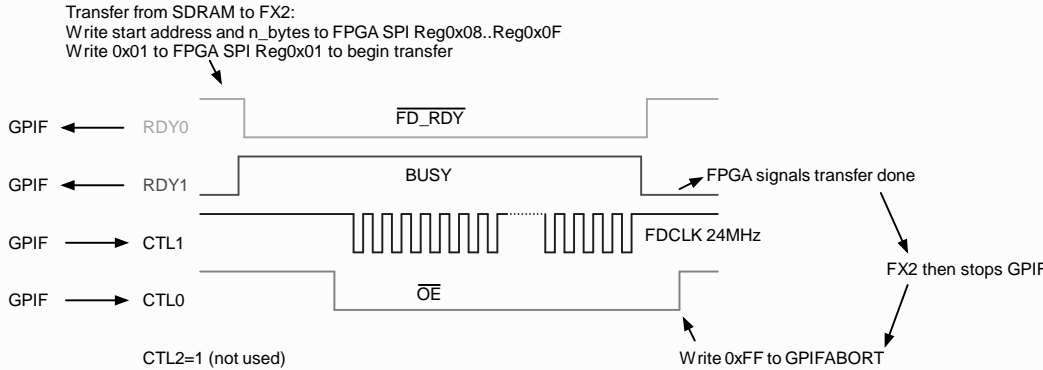
CYPRESS FX2LP USB



For UART communication with authentication IC U10, via the FPGA

^A For FPGA configuration the following signals are used:
SPI_SCLK
SPI_MOSI
FPGA_nCONFIG
FPGA_nSTATUS
FPGA_CONF_DONE

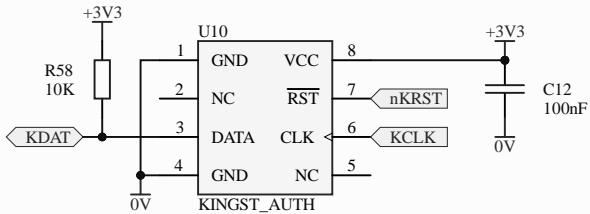
For accessing the control registers in the FPGA the following signals are used:
SPI_SCLK
SPI_MOSI
SPI_MISO
SPI_SS



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FPGA FBGA256 (1mm pitch)

KINGST AUTHENTICATION



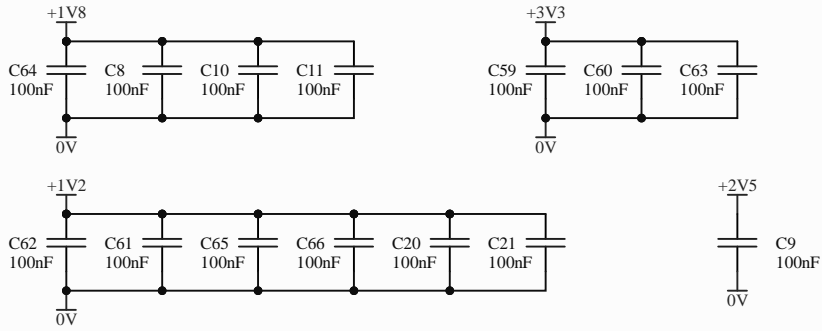
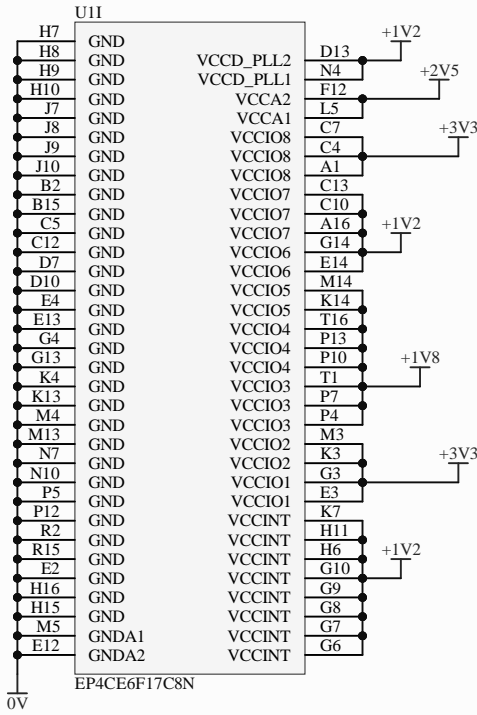
Kingst Authentication IC U10

When the FPGA initialisation completes and it enters run mode, it receives 16 bytes from the 'KAuth' chip. The FPGA uses this to authenticate the bitstream. So, even although the LA1016 and LA2016 are the same hardware, you cannot use the LA2016 bitstream on the LA1016 to boost it to the 200MHz sample rate.

Also, when the KingstVIZ software connects it performs a challenge-response with this IC (via the FPGA) to ensure KingstVIZ can only be used with genuine Kingst LA.

KCLK is 4.8MHz. KDAT is UART protocol 8E1 (even parity) at 12900 baud.

FPGA POWER PINS



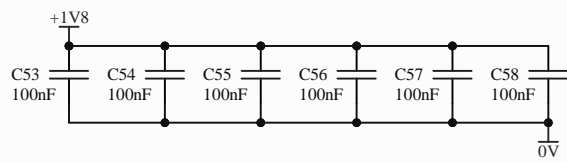
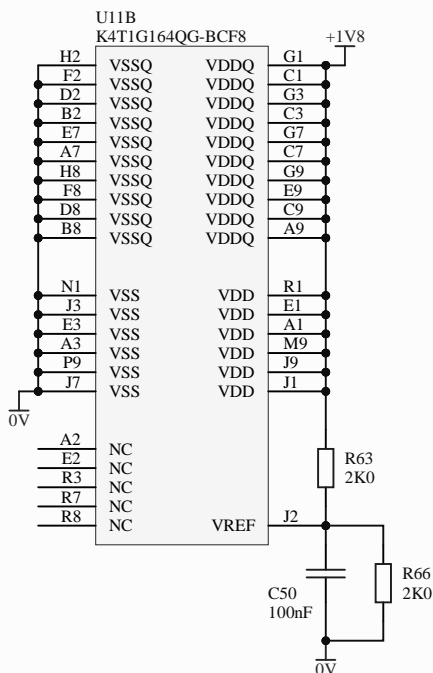
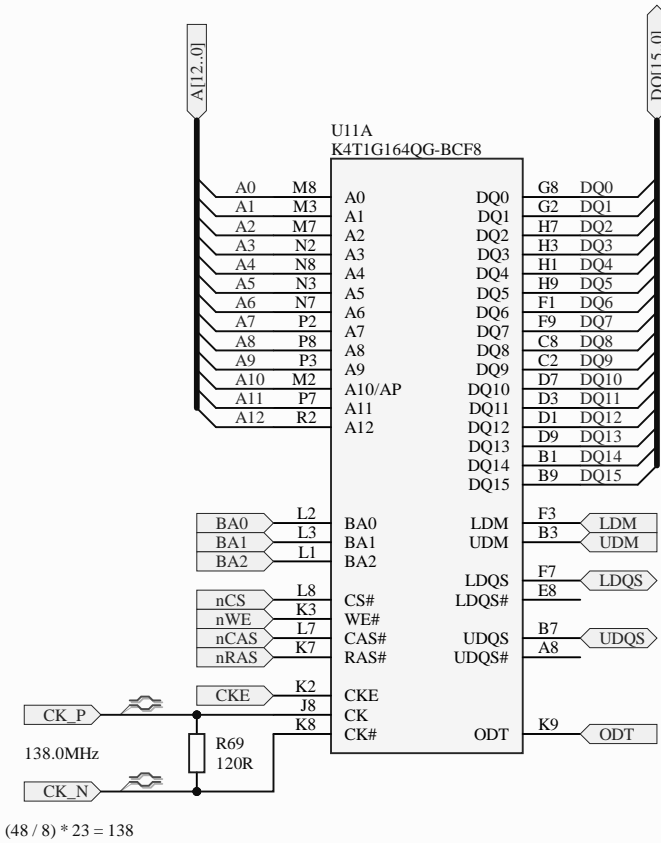
Title **LA1016 / LA2016 PCB V1.3.0**

Size: A3 Number: * Revision: 2

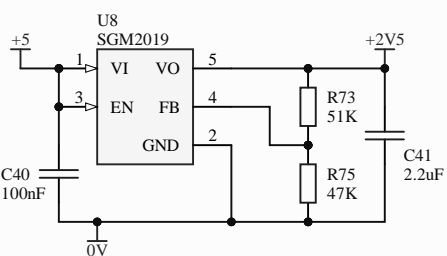
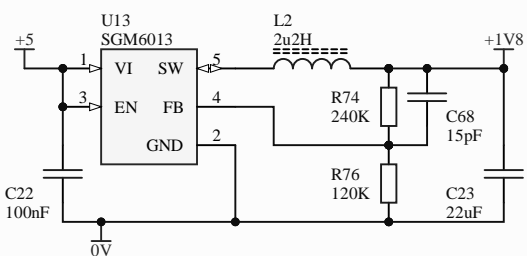
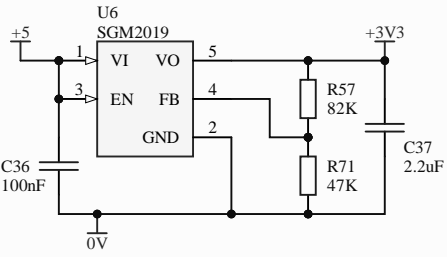
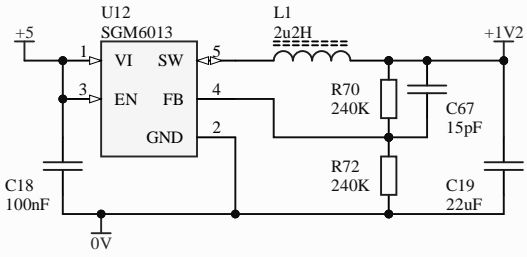
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DDR2 SDRAM 1Gbit FBGA84 x16 (0.8mm pitch)

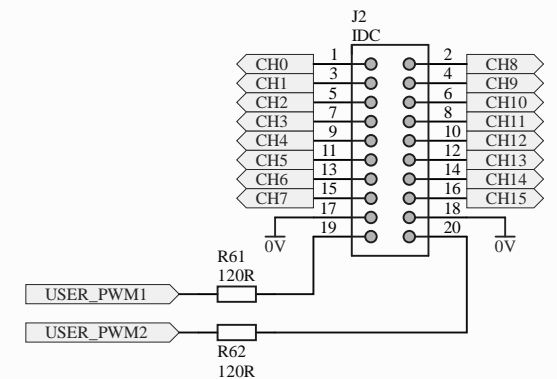
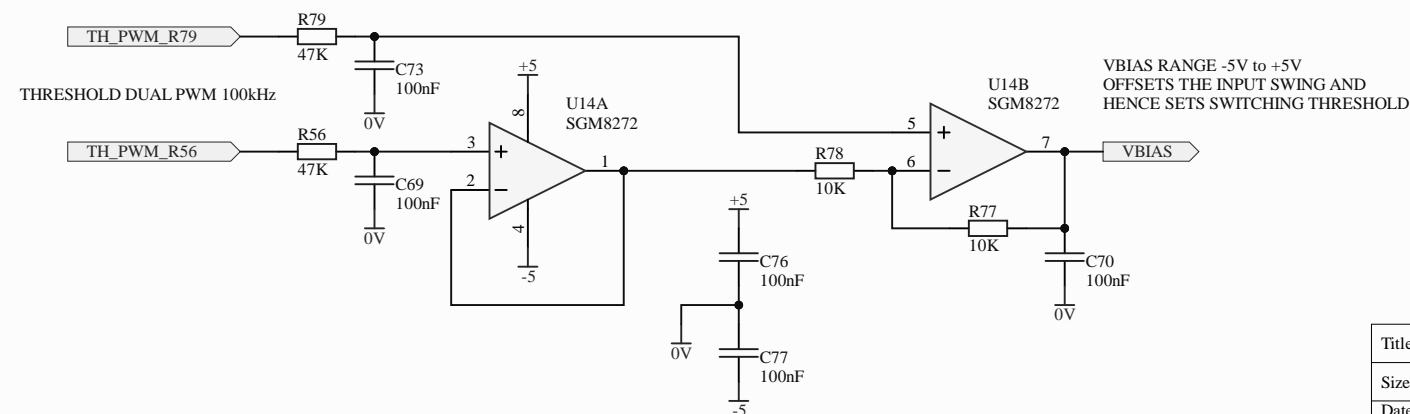
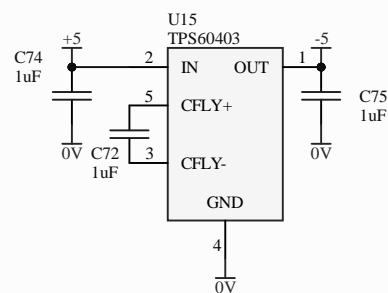
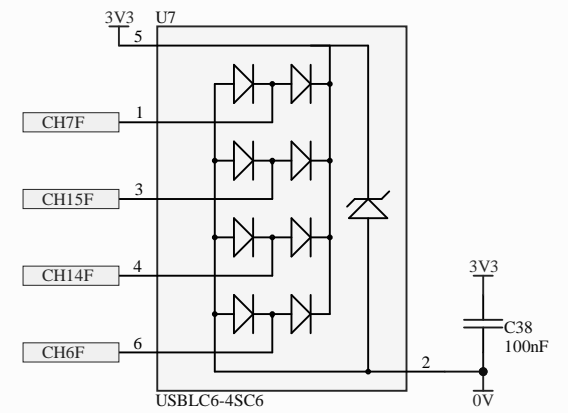
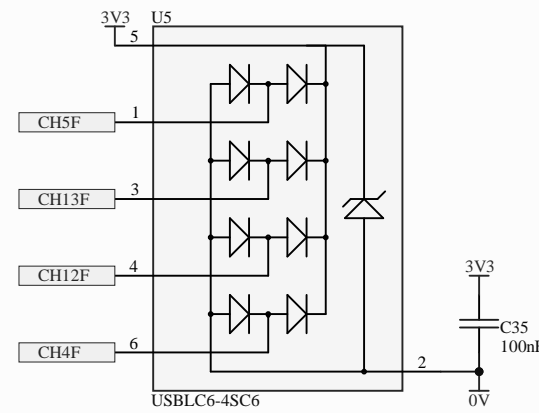
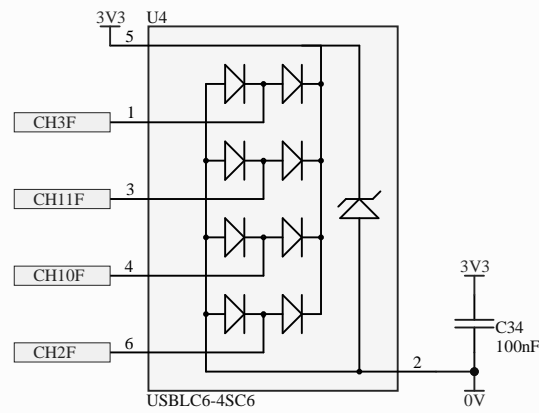
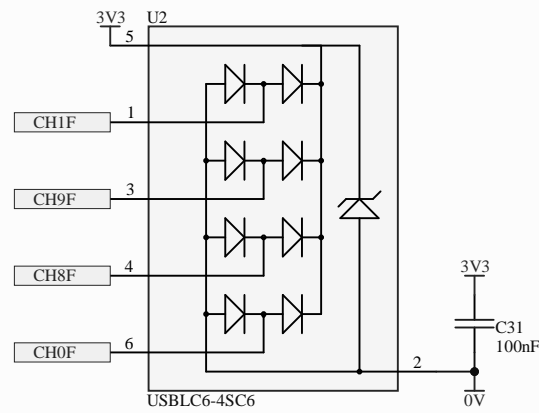
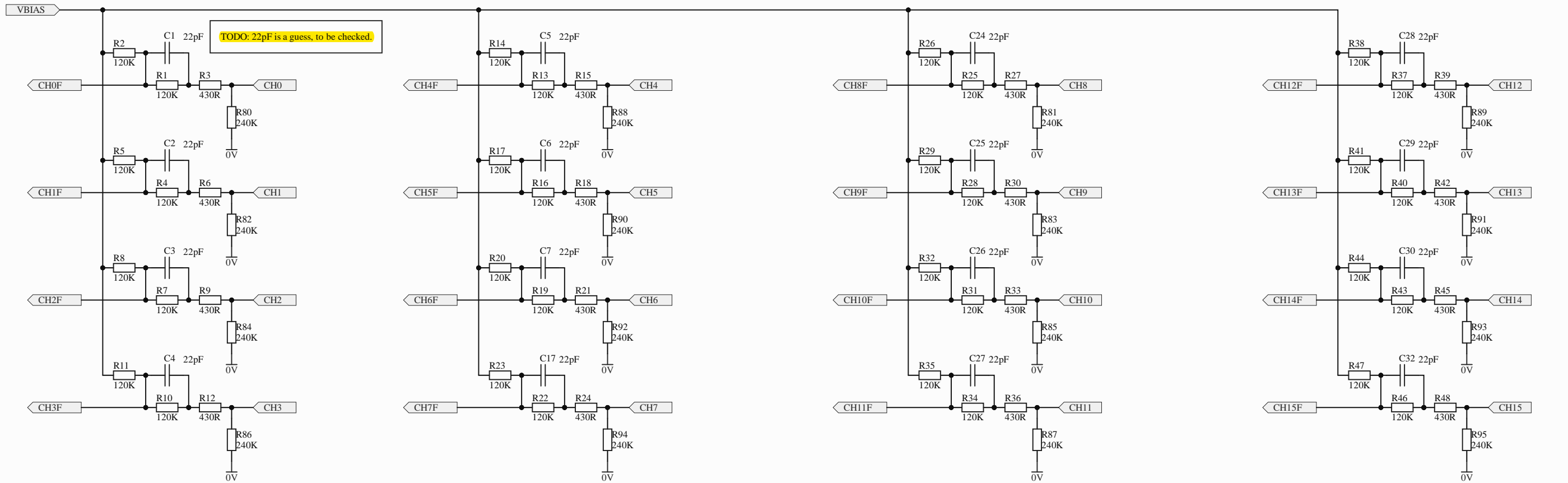


VOLTAGE REGULATORS



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INPUT ATTENUATORS AND THRESHOLD ADJUSTMENT



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Threshold voltage setting in Kingst software versus
VBIAS and FPGA threshold PWM register values

PWM1 = FPGA registers [0x69 0x68] = PWM on R56
PWM2 = FPGA registers [0x6B 0x6A] = PWM on R79

Set (V)	VBIAS (V)	PWM1 hex	PWM2 hex
4.00	-2.822	0350	0000
3.80	-2.630	0313	0000
3.60	-2.430	02D7	0000
3.45	-2.277	02A9	0000
3.30	-2.126	027C	0000
3.15	-1.973	024E	0000
3.00	-1.822	0221	0000
2.91	-1.732	0206	0000
2.90	-1.722	0203	0000
2.80	-1.626	03C9	00F2
2.40	-1.222	0350	00F2
2.00	-0.818	02D7	00F2
1.50	-0.310	023F	00F2
1.00	0.194	01A8	00F2
0.50	0.700	0110	00F2
0.00	1.200	0079	00F2
-0.39	1.600	0003	00F2
-0.40	1.604	03C9	02D7
-0.50	1.705	03AB	02D7
-1.00	2.212	0313	02D7
-1.50	2.716	027C	02D7
-2.00	3.225	01E4	02D7
-2.50	3.728	014D	02D7
-3.00	4.236	00B5	02D7
-3.50	4.740	001E	02D7
-4.00	1.825	FF87*	02D7

* FF87 is overflow error here in Kingst software V3.43
so VBIAS is wrong for this step.

The host software can use these equations to calculate PWM1 register value for a given threshold voltage:

